Table of Contents: Volume 24 (2000)

Number 1

Special Issue on Recent Advances in the Design and Implementation of Signal Processing Systems
Guest Editors: Elias S. Manolakos and Wayne Burleson

Guest Editors' Introduction ..... *Elias S. Manolakos and Wayne Burleson* 5
List of Reviewers 7
Efficient Wordlength Reduction Techniques for DSP Applications ..... *Paul D. Fiore* 9
A Hierarchical Block-Floating-Point Arithmetic ..... *Shiro Kobayashi and Gerhard P. Fettweis* 19
DCT-Domain Embedded Memory Compression for Hybrid Video Coders ..... *Richard P. Kleihorst and René J. van der Vleuten* 31
Design and Implementation of a Low Complexity VLSI Turbo-Code Decoder Architecture for Low Energy Mobile Wireless Communications ..... *Sangjin Hong and Wayne E. Stark* 43
Partitioning Analog and Digital Processing in Mixed-Signal Systems ..... *Sydney Reader, Won Namgoong and Teresa Meng* 59
Linear QR Architecture for a Single Chip Adaptive Beamformer ..... *G. Lightbody, R. Walke, R. Woods and J. McCanny* 67
Multidimensional Exploration of Software Implementations for DSP Algorithms ..... *Eckart Zitzler, Jürgen Teich and Shuvra S. Bhattacharyya* 83
DG2VHDL: A Tool to Facilitate the High Level Synthesis of Parallel Processing Array Architectures ..... *Andrew Stone and Elias S. Manolakos* 99

Numbers 2/3

Special Issue: VLSI on Custom Computing Technology
Guest Editors: Jeffrey Arnold, Wayne Luk and Ken Pocek

Guest Editors' Introduction ..... *Jeffrey Arnold, Wayne Luk and Ken Pocek* 127
Pipeline Reconfigurable FPGAs ..... *Herman H. Schmit, Srihari Cadambi, Matthew Moe and Seth C. Goldstein* 129
Design and Implementation of the MorphoSys Reconfigurable Computing Processor ..... *Ming-Hau Lee, Hartej Singh, Guangming Lu, Nader Bagherzadeh, Fadi J. Kurdahi, Eliseu M.C. Filho and Vladimir Castro Alves* 147
Co-Synthesis to a Hybrid RISC/FPGA Architecture ..... *Maya B. Gokhale, Janice M. Stone and Edson Gomersall* 165
Design-Space Exploration for Block-Processing Based Temporal Partitioning of Runtime Reconfigurable Systems ..... *Meenakshi Kaul and Ranga Vemuri* 181
Application of Reconfigurable CORDIC Architectures ..... *Oskar Mencer, Luc Séméria, Martin Morf and Jean-Marc Delosme* 211
A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition Using Hidden Markov Models ..... *Panagiotis Stogiannos, Apostolos Dollas and Vassilis Digalakis* 223
The CAM-Brain Machine (CBM): Real Time Evolution and Update of a 75 Million Neuron FPGA-Based Artificial Brain ..... *Hugo de Garis and Michael Korkin* 241